REMARKS

## I. Objection to the Drawings

Figure 1 was objected to because it was not noted as being prior art. The applicant has amended the drawing as suggested by the office action.

## II. Claim Objections

The claims were objected to due to misnumbering of new claims. The claim numbering and dependence has been corrected herein.

## III. Rejections of Claims 26-41 Under 35 U.S.C. §103(a)

Claims 26-41 were rejected under 35 U.S.C. §103(a) as being unpatentable over Warn.

CLAIM 26

Claim 26 is independent and recites the following:

> A computer system comprising:
> internal memory; and
> an input/output section;
> wherein the rate of input/output transactions in said input/output section is exponentially related to the amount of internal memory.

The office action is correct in that Warn teaches that input/output transaction response time is exponentially related to internal memory. The office action then states

that the transaction rate is inversely proportional to the transaction's response time. The office action then states that it would have been obvious to relate the transaction rate to the internal memory. The applicant disagrees with this conclusion.

Claim 26 recites "wherein the rate of input/output transactions in said input/output section is exponentially related to the amount of internal memory", which is the number of input/output transactions that may occur over a specific period of time. Warn relates to the response time or the time that the transactions take to occur within the system. A system may have a very long response time, but be able to have many input/output transactions occurring because it is able to operate with the long response time. For example, parallel transactions or cued transaction rates are not affected by the response time after equilibrium is acheived. Thus, the response time and the transaction rate are not necessarily related as suggested by the office action.

Based on the foregoing, the Warn reference does not suggest the exponential relationship between input/output transaction rates and memory as claimed. Therefore, the rejection has been overcome and the applicant requests reconsideration of the rejection.

CLAIMS 27-33

Claims 27-33 are dependent on claim 26 and are deemed allowable by way of their dependence and for other reasons. Therefore, the applicant requests reconsideration of the rejections.

CLAIM 34

Claim 34 is independent and recites the following:

> A method for manufacturing a computer system, said method comprising:

proving internal memory for said computer system; and

providing an input/output section for said computer system, wherein said input/output section has an input/output transaction rate associated therewith;

wherein said input/output transaction rate is exponentially related to the amount of said internal memory.

Claim 34 was rejected on the same grounds as claim 26. Therefore, the applicant asserts that the response time of Warn is not related to the input/output transaction rate of claim 34.

Therefore, the rejection has been overcome and the applicant requests reconsideration of the rejection.

CLAIMS 35-41

Claims 35-41 are dependent on claim 34 and are deemed allowable by way of their dependence and for other reasons. Therefore, the applicant requests reconsideration of the rejections.

In view of the foregoing, all pending claims are in condition for allowance and a notice to that effect is requested.

Respectfully submitted,
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